



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/877,371	06/08/2001	Benjamin Edward Russ	68581	2434

22242 7590 02/04/2004

FITCH EVEN TABIN AND FLANNERY
120 SOUTH LA SALLE STREET
SUITE 1600
CHICAGO, IL 60603-3406

EXAMINER

HARPER, HOLLY R

ART UNIT	PAPER NUMBER
----------	--------------

2879

DATE MAILED: 02/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/877,371

Applicant(s)

RUSS ET AL.

Examiner

Holly R. Harper

Art Unit

2879

fw

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 June 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). ____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____ 6) ☐ Other:

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Claims 1 and 2 mention electron emitter lines contained within an in-laid isolation barrier. The drawings do not show more than one emitter line per trench. Therefore, multiple electron emitter lines per trench must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 2, 6, 8, 9, 12, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuo (USPN 5,340,997).

In regard to claim 1, the Kuo reference discloses a field emission device with a substrate (Figure 1A, Element 102) and an isolation barrier (trench) formed within the top surface of the

Art Unit: 2879

substrate, which contains an emitter line (Figure 1A, Element 108). The substrate is made of insulating material (Column 5, Line 68- Column 6, Line 2), which provides field isolation between the emitter lines. While Kuo exemplifies a single emitter, it is within the Kuo teachings the use of a multiple emitters to create a large-scale FED.

The phrase “adapted to” suggests or makes optional but does not limit a claim to a particular structure and does not limit the scope of a claim or claim limitations. Therefore, the limitation “adapted to contain electron emitter lines” has not been given patentable weight. See MPEP 2106 (c).

In regard to claim 2, the Kuo reference discloses that an electron emitter line is formed within the isolation barrier (Figure 1A, Element 108).

In regard to claim 6, the Kuo reference discloses that the in-laid linear isolation barrier is a trench (Figure 1A, Element 108).

In regard to claim 8, the Kuo reference discloses that the isolation barrier extends the length of the substrate (Figure 1A).

In regard to claim 9, the Kuo reference discloses a field emission device with a substrate (Figure 1A, Element 102) and an isolation barrier (trench) formed within the top surface of the substrate, which contains an emitter line (Figure 1A, Element 108). The substrate is made of insulating material (Column 5, Line 68- Column 6, Line 2), which provides field isolation between the emitter lines. While Kuo exemplifies a single emitter, it is within the Kuo teachings the use of a multiple emitters to create a large-scale FED.

In regard to claim 12, the Kuo reference discloses that each emitter line is a separate and discrete continuous lines extending across the substrate (Figure 1A).

Art Unit: 2879

In regard to claim 15, the Kuo reference discloses an emitter line (Figure 1A, Figure 108) within an in-laid isolation barrier (Figure 1A). The emitter line is one continuous piece and there are no separating structures positioned between adjacent emitter portions on the surface within the in-laid isolation barrier (Figure 1A).

4. Claims 1, 2, 6, 12, and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jones et al. (USPN 6,027,388)

In regard to claims 1, 2, and 12, the Jones reference discloses a field emission device with a cathode substrate (Figure 6, Element 100) and an isolation barrier formed within the top surface of the substrate, which contains an emitter tip (Figure 6, Element 510). The insulating substrate can be formed of glass or ceramic (Column 1, Lines 37-42) and provides field isolation between the emitter lines (Figure 6). The Jones reference discloses that various emitter shapes can be used (Column 1, Lines 25-30), but does not specifically disclose the use of an emitter line. However, it is noted that the inclusion of a line emitter is not shown to solve any problems or yield any unexpected results that are not within the scope of Jones's FED. Flat emitter lines are cheaper than cone emitters and easier to make uniform on a large scale substrate plate. The emitter lines would take the place of the emitter tips. Therefore, the in-laid barriers would now surround the emitter lines instead of emitter tips. Thus, it would have been obvious at the time the invention was made to a person having ordinary skills in the art to incorporate flat emitter lines, instead of emitter tips.

In regard to claim 6, the Jones reference discloses that the isolation barriers comprise one or more trenches (Figure 6).

In regard to claim 15, the Jones reference discloses an emitter line (Figure 6, Figure 510) within an in-laid isolation barrier (Figure 6). The emitter line is one continuous piece and there are no separating structures positioned between adjacent emitter portions on the surface within the in-laid isolation barrier (Figure 6).

In regard to claim 16, the Jones reference discloses that the trenches are designed to contain electron emitters for emitting electrons to a display screen (Column 1, Lines 21-40).

In regard to claim 17, the Jones reference discloses a gate structure (Figure 6, Element 410) that causes electron emission from an emitter line to a display screen (Column 1, Lines 21-40).

5. Claims 3, 7, 11, and 14 rejected under 35 U.S.C. 103(a) as being unpatentable over Jones et al. (USPN 6,027,388) in view of Novich (USPN 5,811,926).

In regard to claims 3 and 7, the Jones reference discloses an FED with in-laid isolation means, but does not disclose the use of a gate wire frame. The Novich reference teaches that a gate wire frame with gate wires made of aluminum fibers is used to space apart the cathode and anode assembly. The Novich reference discloses spacers (gate wires) made of aluminum fibers (Column 9, Lines 48-51) in a frame (Figure 11) positioned over the substrate (Figure 2, Element 616). This spacer design allows for a stable, self-leveling design that reduces cost and waste during FED assembly (Column 2, Lines 12-25).

Regarding claims 3 and 7, the recitation “dampen vibrations in the gate wires due to the driving frequency” has not been given patentable weight because is considered an intended used recitation. It has been held that a recitation with respect to the manner in which a claimed

Art Unit: 2879

apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations.

In regard to claim 11, the Jones in view of Novich reference discloses that a top portion of the isolation barriers are adapted to contact a gate structure extending over the isolation barriers (Figure 2, Element 570 and 616) and (Figure 11).

In regard to claim 14, the Jones in view of Novich reference discloses a gate structure extending over the isolation barriers (Figure 2 and 11).

6. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuo in view of Chason (USPN 5,019,003).

In regard to claim 1, the Kuo reference discloses a field emission device with a substrate (Figure 1A, Element 102) and an isolation barrier (trench) formed within the top surface of the substrate, which contains an emitter line (Figure 1A, Element 108). The substrate is made of insulating material (Column 5, Line 68- Column 6, Line 2), which provides field isolation between the emitter lines. While Kuo exemplifies a single emitter, it is within the Kuo teachings the use of a multiple emitters to create a large-scale FED.

In regard to claims 4 and 5, the Kuo reference does not disclose that a trace is used to connect the top surface of the substrate to the emitter line. The Chason reference teaches that a field emission device can have a trace between the substrate and the emitter. This will help control the surface potential. The trace would need to be bent to reach between the substrate and into the trench where the emitter is located. Thus, it would have been obvious at the time the invention was made to a person having ordinary skills in the art to incorporate a trace between the substrate and the emitter, as taught by Chason.

Art Unit: 2879

7. Claims 9, 10, 13, and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Novich (USPN 5,811,926).

In regard to claim 9, the Novich reference discloses a field emission device with a cathode substrate (Figure 2, Element 530 and 542) and an isolation barrier formed within the top surface of the substrate, which contains an emitter tip (Figure 2, Element 556 and 570). The substrate has a conductive layer on top of its substrate, making this the top layer of the substrate (Figure 2, Elements 530 and 542). The conductive layer is made of row conductors (Column 5, Lines 24-30), parts of which are coated with insulative material to make insulating barriers (Column 6, Lines 20-24). The emitters are between the barriers (Figure 2) and are therefore in-laid in the top surface of the substrate. The insulating substrate can be formed of glass or a polymeric material (Column 4, Lines 56-58) and provides field isolation between the emitter lines. The Novich reference discloses the use of a row of cone emitters, but does not disclose the use of an emitter line. However, it is noted that the inclusion of a line emitter is not shown to solve any problems or yield any unexpected results that are not within the scope of Jones's FED. Flat emitter lines are cheaper than cone emitters and easier to make uniform on a large scale substrate plate. The emitter lines would take the place of the emitter tips. Therefore, the in-laid barriers would now surround the emitter lines instead of emitter tips. Thus, it would have been obvious at the time the invention was made to a person having ordinary skills in the art to incorporate flat emitter lines, instead of emitter tips.

In regard to claim 10, the Novich reference discloses spacers (gate wires) made of aluminum fibers (Column 9, Lines 48-51) in a frame (Figure 11) positioned over the substrate (Figure 2, Element 616). The recitation "dampen vibrations in the gate wires due to the driving

Art Unit: 2879

frequency” has not been given patentable weight because is considered an intended used recitation. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations.

In regard to claim 13, the Novich reference discloses that the in-laid means support the gate structure (Figure 2, Element under Element 584) and the gate structure extends over the linear in-laid means (Figure 11).

In regard to claim 18, the Novich reference discloses separate in-laid means deposited on a surface (Figure 2, the Element under Element 584). As explained above, emitter lines could be used instead of emitter cones. With the use of emitter lines, there would be no separating structure between adjacent emitter portions.

In regard to claim 19, the Novich reference discloses that linear in-laid isolation means (Figure 2, Element under Element 584) for isolating linear electron fields emitted from adjacent emitter lines to a display screen (Figure 2, Element 568).

In regard to claim 20, the Novich reference discloses means for causing electron emission from an emitter line to a display screen (Figure 2).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Jones et al. (USPN 6,136,621) discloses that the emitters in FEDs can be cone or line emitters.

Goel et al. (USPN 6,486,597) discloses that the emitters in FEDs can be cone or line emitters.

Response to Arguments

8. Applicant's arguments filed 11/10/2003 have been fully considered but they are not persuasive:

Regarding applicants claim that Kuo does not disclose multiple emitter lines, the examiner respectfully agrees. While Kuo exemplifies a single emitter, it is within the Kuo teachings that multiple emitters are used to create a large-scale FED. See Column 3, Lines 30-35 and Column 7, Lines 1-8.

Regarding applicants claim that Kuo does not disclose how the trench would provide field isolation between the emitter lines, the examiner respectfully disagrees. Kuo discloses that the electrons are emitted from the tip of the emitter (Figure 2). The design of the emitter and substrate allows the insulating substrate to insulate the emitter. The electrons are emitted from the tip of the emitter and then directed. Obviously the substrate is insulating the emitter.

Regarding applicants claim that there is no motivation to combine Novich with Kim, the examiner respectfully agrees. However, the examiner believes the use of emitter lines instead of emitter cones is a matter of design choice. The use of emitter lines provides advantages over emitter cones. The geometry of the spacer unit disclosed by Novich would block some of the emission of electrons to the display, but only in areas where emission is not desired.

Art Unit: 2879

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Holly Harper whose telephone number is (571) 272-2453. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimesh Patel, can be reached on (571) 272-2457. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7382.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.



Holly Harper
Patent Examiner
Art Unit 2879



NIMESHKUMAR D. PATEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800